IN THE CLAIMS:

Please cancel without prejudice claims 1 – 9, 16 – 26, 27 – 34, 37 – 42, 46 – 49, 60, 61 – 62, 64, 65, 66 – 86, 87 – 94, and 95 – 97, respectfully.

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1. - 42. (Canceled)

43. (Previously Presented) A system comprising:

a central processing unit with associated register file; and

a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator marks the variables in the native CPU register file as modified when updated by the execution of Java byte codes.

44. (Previously Presented) The of claim 43, wherein the hardware accelerator copies the variables marked as modified to the system memory for some bytecodes.

45. (Previously Presented) The system of Claim 44, wherein at least portions of the hardware accelerator are part of the CPU.

46.- 49. (Canceled)

50. (Previously Presented) A system comprising:

a central processing unit with associated register file; and

a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator generates a new Java PC due to a "GOTO" or "GOTO_W" byte code.

51. (Previously Presented) The system of Claim 50, wherein at least portions of the hardware accelerator are part of the CPU.

52. (Previously Presented) A system comprising:

a central processing unit with associated register file; and

a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator generates a new Java PC due to a "JSR" or "JSR_W" byte code, computes the return Java PC and pushes the return Java PC on to the operand stack.

53. (Previously Presented) The system of Claim 52, wherein at least portions of the hardware accelerator are part of the CPU.

54. (Previously Presented) A system comprising:

a central processing unit with associated register file; and

a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator sign extends the SiPush and Bipush byte codes and appends to the immediate filed of the native instruction being composed.

55. (Previously Presented) The system of Claim 54, wherein at least portions of the hardware accelerator are part of the CPU.

56. (Previously Presented) A system comprising:

a central processing unit with associated register file; and

a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator sign

extends the SiPush and Bipush byte codes and made available to be read by the native CPU.

57. (Previously Presented) The system of Claim 56, wherein at least portions of the hardware accelerator are part of the CPU.

58. (Previously Presented) A system comprising:

a central processing unit with associated register file; and

a hardware accelerator operably connected to the central processing unit, the hardware accelerator adapted to convert stack-based instructions into register-based instructions native to the central processing unit, where the hardware accelerator increments the Java PC within the hardware accelerator by generating an increment value based on the number of byte codes being disposed, wherein the Java PC is incremented in the correct manner if multiple bytecodes are disposed at the same time .

59. (Previously Presented) The system of Claim 58, wherein at least portions of the hardware accelerator are part of the CPU.

60.- 62. (Canceled)

63. (Previously Presented) A system comprising;

a first unit adapted to execute register-based instructions;

a hardware unit associated with the first unit, the hardware unit adapted to decode stack-based instructions, store operands for stack based instructions in the first units register file wherein an underflow or overflow indication is produced for the portion of the operand stack stored in the register file; the hardware unit causing execution of the stack based instructions by the first unit's execution unit.

64.-100. (Canceled)

101. (Previously Presented) A system comprising a first unit adapted to have at least an execution unit, a hardware unit associated with the first unit, the hardware unit adapted to decode stack-based instructions and execute said instructions using the execution unit wherein at least some of the stack based instructions executed are branch instructions and at least some of the stack-based instructions cause an exception whereby they are executed in software.

102. (Previously Presented) The system of claim 101 wherein at least some of the Java registers are maintained in hardware.

103. (Previously Presented) The system of claim 101 wherein at least some of the stack-based instructions are from a cache

104. (Previously Presented) The system of claim 101 wherein the branch instructions for java byte codes includes at least one of ifeq, ifne, iflt, ifge, ifgt, ifle, if_icmpeq, if_icmpne, if_icmplt, if_acmpge, if_cmpgt, if_icmple, if_acmpeq, if_acmpne, ifnull, ifnonull, lcmp, fcmpl, fcmpg, dcmpl, or dcmpg.

105. (Previously Presented) The system of claim 101 wherein the execute logic produces a branch indication for at least some of the branch instructions.

106. (Previously Presented) The central processing unit of claims 64, 66, 69, 71, 72,73,76,80,81,83, 84, 86, 95 and 98 where the stack-based instructions are Java byte codes.

107. (Previously Presented) The system of claims 63, 65, and 101 where the stack-based instructions are Java byte codes.

108. (Previously Presented) The system of claims 63, 65, and 101 where the hardware unit is part of the central processing unit.